ctrlX - CORE

• ctrlX I/O

- Configuration of the ctrlX I/O
- Annex: Communication ctrlX < == > XM
- ctrlX sample program
- XM sample program

Jordi Laboria (DCET/SLF4-ES)





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ctrlX - Configuration of the ctrlX I/O

GOALS:

- Configuration of the I/O Modules (Digital Inputs / Outputs)
- Modbus communication for input control and output activation from the XM







Configuration of the ctrlX I/O

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Connection of the EtherCat Bus Coupler



The NET status LED is specified by the ETG (EtherCAT Technology Group) and indicates the EtherCAT bus state at the bus coupler.

The operating state is displayed in green ^{GN}:

LED color green	Description
Off	Status INIT
Flickers	Status BOOT
Flashes	Status PRE-OP
Single flash	Status SAFE-OP
Lit	Status OP

The error state is displayed in red **RD**:

LED color red	Description
Off	No error
Flickers	Boot error
Flashes	Invalid configuration
Single flash	Local error (e.g. synchronization)
Double flash	Watchdog error
Lit	Communication error



Both connections are required



In the example we will use the following configuration



J				
Sinn-II	1 - DI CH.	1	Grey	
	2 - DI CH.	2	Grey	
(3 - DI CH.	3	Grey	
	4 - DI CH.	4	Grey	
	5 - DI CH.	5	Grey	
	6 - DI CH.	6	Grey	
Ъůр	7 - DI CH.	7	Grey	
Щ.	8 - DI CH.	8	Grey	
Жğн	9 - DI CH.	9	Grey	
XQ:	10 - DI CH	1.10	Grey	
<u>m</u>	11 - DI CH	1.11	Grey	
	12 - DI CH	1.12	Grey	
(#	13 - DI CH	1.13	Grey	
	14 - DI CH	1.14	Grey	
	15 - DI CH	1.15	Grey	
	16 - DI CH	1.16	Grey	
Ţ	Assignment	Color		Max. current
		Crow		0.5.4
O DC	1 - DO CH.1	Grey		0.5 A
œ.	1 - DO CH.1 2 - DO CH.2	Grey Grey		0.5 A 0.5 A
	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3	Grey Grey Grey		0.5 A 0.5 A 0.5 A
	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5	Grey Grey Grey Grey		0.5 A 0.5 A 0.5 A 0.5 A
	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6	Grey Grey Grey Grey Grey		0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A
₿₿₽	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.4 6 - DO CH.6 7 - DO CH.7	Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A
	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A
	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8 9 - DO CH.9	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A 0.5 A
₿₿₽₽₽₽₽₽₽₽₽₽	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8 9 - DO CH.9 10 - DO CH.10	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A
₿₿₿₿₿₿₿₿₿	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8 9 - DO CH.9 10 - DO CH.10 11 - DO CH.11	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A
₿₿₽₽₽₽₽₽₽₽₽₽₽₽	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8 9 - DO CH.8 9 - DO CH.9 10 - DO CH.10 11 - DO CH.11 12 - DO CH.12	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A
▋₿₿₿₿₿₿₿₿₿₿₿₿₿₿₿	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8 9 - DO CH.9 10 - DO CH.9 10 - DO CH.10 11 - DO CH.11 12 - DO CH.12 13 - DO CH.13	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A
<u>╞</u> ╞╞╒╤╤╤╤╤	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.8 9 - DO CH.9 10 - DO CH.9 10 - DO CH.10 11 - DO CH.11 12 - DO CH.13 14 - DO CH.14	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A
	1 - DO CH.1 2 - DO CH.2 3 - DO CH.3 4 - DO CH.4 5 - DO CH.5 6 - DO CH.6 7 - DO CH.7 8 - DO CH.9 10 - DO CH.9 10 - DO CH.10 11 - DO CH.11 12 - DO CH.12 13 - DO CH.13 14 - DO CH.15	Grey Grey Grey Grey Grey Grey Grey Grey		0.5 A 0.5 A

Color

The "Device State" signals are identical in all the devices

Device state	LED flashing pattern
Booting	BU BU BU BU
Initialization	BU BU BU BU BU BU BU BU BU 🖶
It is currently configured. Module not yet ready.	gn gn gn gn gn
Process data transmission, outputs inactive.	gn gn gn gn gn gn gn gn 🗂 🕳
Module in "Run" state	gn 🕁
Error and warning states	
Logic or peripheral voltage error	RD RD RD RD RD RD RD RD RD 🕁
Communication or configura- tion error	RD RD RD RD



The next step will be to proceed to enter the configuration from the Software.

The first screen that will open will show us the equipment that we have generated, virtual or real systems if we are connected to any of the equipment, in the image a ctrlX-Core appears in "State" Online, which is the one we are using for tests

WORKS	ctrlX WORKS $ imes$	Devices				en • ② rexroth
	曲 Devices					^
ctrIX WORKS NRK-V-0114.	📰 Engineering Tools	ctrlX WOR	KS			
1	🖭 App Build Environments	Device overview	d engineering			
		Find the ctrlX CORE hardware in hardware.	the network or add a ctrlX COREvi	rtual and develop your applications - even without	Navigate to the ctrLX COF engineering.	RE or ctrlX COREvirtual homepage and start
		Go to documentation				
		2 items				5 +
		Name	State	Туре	IP addresses	Actions
		VirtualControl-1	Offline	ctrlX CORE ^{virtual}		
		ctrlX-CORE	Online	ctrlX CORE	192.168.1.1	9
					1	



If we connect, clicking on the "IP addresses" will open another menu in which we will be asked for the Password for the connection, which will open the connection from the part of the browser that we have preset in the system.



By default the first connection can be made using the default "UserName" and "Password"

The usage of the ctrIX CORE^{virtual} is limited to development, evaluation and simulation. Operative usage is not intended.



Username		
boschrexroth	boschrexroth	
The initial username	is: boschrexroth	
Password		
•••••	<i>boschrexroth</i>	\odot
The initial password	is: boschrexroth	
✓ I accept the	General Terms of Use.	
		Login

This displays the generic menu, from which we can access all the available elements. The screen may vary depending on the software version used



After this first connection, the system will ask us to modify the "Password", which must include a minimum of 12 digits, including numbers and capital letters, the "Username" does not need to be changed.





We go back one step and from the Software we will choose the "Engineering Tools" option and within this we will activate the "Open ctrlX I/O Engineering" option





We can also access from the browser, accessing the "EtherCAT" menu







Once in the system we must, if not, incorporate the "EtherCat Master"



Then we must scan the equipment

The ''scanned'' equipment appears on the right and we proceed to insert the new elements



After this, the found equipment also appears on the left and we can proceed to "Apply" or directly "OK"

🖳 Project			🛅 Control		
Device name	Device type		Device type	Vendor	
▲ 🔲* XB_EC_12	XB-EC-12 Bus coupler Pwrln UL UP		🔺 🔲 XB-EC-12 Bus coupler Pwrln UL UP	Bosch Rexroth AG	
🔺 🚡 * XF71	XF71	-	🔺 🍐 XF71		
XI110116	XI110116 16Ch. Dig. Input 24V, 3ms		XI110116 16Ch. Dig. Input 24	Bosch Rexroth AG	
XI110116_1	XI110116 16Ch. Dig. Input 24V, 3ms	_	XI110116 16Ch. Dig. Input 24	Bosch Rexroth AG	
XI211116	XI211116 16Ch. Dig. Output 24V/		XI211116 16Ch. Dig. Output 2	Bosch Rexroth AG	
XI211116_1	XI211116 16Ch. Dig. Output 24V/		XI211116 16Ch. Dig. Output 2	Bosch Rexroth AG	
		*			
		\Diamond	OK Cancel	Apply	Help

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ctrlX - Configuration of the ctrlX I/O - Scan I/O modules

Now all the new modules appear under the "EtherCat Master"





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All modules have associated menus, in general, activating the "Expert Settings" more menus are displayed. In the example we see the first input module.

XI110116 (XI110116 16Ch. Dig. Input 24V, 3ms)			General Sync	Manager Expe	ert Process Data Pro	ocess Data Online	ESC 🛛 🗮 EtherCAT I/O Mapping 🌒 Information
General Process Data Online 🗮 EtherCAT I/O Mapping 🊺 Information			Address — AutoIncad	dress -2	A	— Additional —	Ether CAT
Address Additional Additional	Ether CAT.		EtherCAT a	ddress 10 d Clock —	03	U Doportsea	
Distributed Clock			 Startup Ch Watchdog 	necking —		▷ Timeouts -	
			Identification Disabled Configure 	n	(ADO 0x0012)	Value	1003
			 Explicit de Data Word 	vice identificati d (2 Bvtes)	ion (ADO 0x0134)	ADO (hex)	16#0
If we enter the "EtherCat I/O Mapping" menu we can see the assigned I/O areas							
🗮 EtherCAT I/O Mapping		Value	%IX10.0	BIT	Value		From my point of view, the I/O areas hould be in the same range to avoid
XI110116 (XI110116 16Ch. Dig. Input 24V, 3ms)		Value	🚺 %IX12.0	BIT	Value		onfusion, regardless of the elements o ach I/O unit. We will modify the initia
XI110116_1 (XI110116 16Ch. Dig. Input 24V, 3ms)		Value	%QX0.0	BIT	Value	a b	reas of each group, to respect the orde oth in the Inputs and in the Outputs.
x1211116_1 (X1211116 16Ch. Dig. Output 24V/0.5A)		Let 1			L		

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The modification will be made from this section, modifying the first of the bytes, assuming the system, the modification of the rest automatically.



Input Mapping

-	$\forall a riable = = = = = = = = = = = = = = = = = = =$	-Map pi n g =	=Ghannel= :	=Address= =	= Ty pe= =	= U nit= =	=Description= == =	= Variable =	= Mapping _	- Channel -	Address =	- Jype —	±Unit=	- Description
-	(🍽		Value	%IX10.0	BIT		Value	*		Value	🚺 %IX12.0	BIT		Value
"	** * }=======		Value	%IX10.1	BIT		Value	╞═╇╤═══╸		Value	%1X12.1	BT		Value — —
	🍫		Value	%IX10.2	BIT		Value	- * *		Value	%IX12.2	BIT		Value
	🍫		Value	%IX10.3	BIT		Value	🍫		Value	%IX12.3	BIT		Value
	¥ø		Value	%IX10.4	BIT		Value	* >		Value	%IX12.4	BIT		Value
	🍫		Value	%IX10.5	BIT		Value			Value	%IX12.5	BIT		Value
			Value	%IX10.6	BIT		Value	* >		Value	%IX12.6	BIT		Value
	🍫		Value	%IX10.7	BIT		Value	🍫		Value	%IX12.7	BIT		Value
	···· *>		Value	%IX11.0	BIT		Value	*		Value	%IX13.0	BIT		Value
			Value	%IX11.1	BIT		Value	🍫		Value	%IX13.1	BIT		Value
	*		Value	%IX11.2	BIT		Value	¥ø		Value	%IX13.2	BIT		Value
	- ×		Value	%IX11.3	BIT		Value			Value	%IX13.3	BIT		Value
	···· *		Value	%IX11.4	BIT		Value	*		Value	%IX13.4	BIT		Value
	· · · · · · · · · · · · · · · · · · ·		Value	%IX11.5	BIT		Value	* >		Value	%IX13.5	BIT		Value
	· · · · · · · · · · · · · · · · · · ·		Value	%IX11.6	BIT		Value	* >		Value	%IX13.6	BIT		Value
	• •		Value	%TX11.7	BIT		Value	- · · · · · · · · · · · · · · · · · · ·		Value	%IX13.7	BIT		Value
	¥		Y CHOIC	/01/11/	011		YORGE	1						

YariableN	tapping _ Channe	L _ Address		 Description	 Variable	Mapping	<u>Channel</u>	<u>Address</u>	Туре	Unit	Description_
│ <u>└──[™]∕∕</u>	Value	M %QX10.0	BIT	Value	 `_		Value	%QX12.0	BIT		Value
- F ø	Value	%QX10.1	BIT	Value	 - * ø		Value	%QX12.1	BIT		Value
*	Value	%QX10.2	BIT	Value	*		Value	%QX12.2	BIT		Value
* ø	Value	%QX10.3	BIT	Value	^K ø		Value	%QX12.3	BIT		Value
*	Value	%QX10.4	BIT	Value	* @		Value	%QX12.4	BIT		Value
* @	Value	%QX10.5	BIT	Value	**		Value	%QX12.5	BIT		Value
*	Value	%QX10.6	BIT	Value	* @		Value	%QX12.6	BIT		Value
* @	Value	%QX10.7	BIT	Value	**		Value	%QX12.7	BIT		Value
*	Value	%QX11.0	BIT	Value	* @		Value	%QX13.0	BIT		Value
^K ø	Value	%QX11.1	BIT	Value	* ø		Value	%QX13.1	BIT		Value
^K ø	Value	%QX11.2	BIT	Value	*		Value	%QX13.2	BIT		Value
* @	Value	%QX11.3	BIT	Value	**		Value	%QX13.3	BIT		Value
*	Value	%QX11.4	BIT	Value	* @		Value	%QX13.4	BIT		Value
^K ø	Value	%QX11.5	BIT	Value	* @		Value	%QX13.5	BIT		Value
[*] @	Value	%QX11.6	BIT	Value	*		Value	%QX13.6	BIT		Value
	Value	%QX11.7	BIT	Value	i 🍫		Value	%QX13.7	BIT		Value

Output Assignment







Online Connection ctrlX

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Assuming that we already have the configuration of the modules prepared, we are going to incorporate this in the part of the PLC program (Codeys)











Once the PLC application is open, we will proceed to verify the connection with the equipment.





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With the established communication we will go on to incorporate the I/O unit to the "DataLayer_Realtime"







When inserting the "Real Time Node" the module that we had previously sent from the I/O configuration already appears



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ctrlX - Configuration of the ctrlX I/O – Online Connection

Before sending the configuration, I recommend reviewing the I/O areas, since many times an unwanted "scrolling" of areas occurs at the moment in which the modules "appear" in the "DataLayer_RealTime"

DataLayerNode I/O Mapping Configuring the inputs in the ''Data Layer Real Time''			Configuration of the previously defined inpu the ctrlX I/O Engineering				trlX I/O Engineering				
Variable	Mapping	Channel	Address	Туре	Variable	Mapping	Channel	Address	Туре	Unit	Description
r 🍫		Channel_1.Value	%IX8.6	BIT	*		Value	%IX10.0	BIT		Value
¥ø		Channel_2.Value	%IX8.7	BIT			Value	%IX10.1	BIT		Value
¥ø		Channel_3.Value	%IX9.0	BIT	*		Value	%IX10.2	BIT		Value
🍫		Channel_4.Value	%IX9.1	BIT	* >		Value	%IX10.3	BIT		Value
*		Channel_5.Value	%IX9.2	BIT	* >		Value	%IX10.4	BIT		Value
🍫		Channel_6.Value	%IX9.3	BIT	* >		Value	%IX10.5	BIT		Value
****		Channel_7.Value	%IX9.4	BIT	* >		Value	%IX10.6	BIT		Value
		Channel_8.Value	%IX9.5	BIT	* >		Value	%IX10.7	BIT		Value
*		Channel 9.Value	%IX9.6	BIT	* >		Value	%IX11.0	BIT		Value
		Channel 10.Value	%IX9.7	BIT	🐌		Value	%IX11.1	BIT		Value
		Channel 11.Value	%IX10.0	BIT	* >		Value	%IX11.2	BIT		Value
		Channel 12.Value	%IX10.1	BIT	*>		Value	%IX11.3	BIT		Value
		Channel 13.Value	%IX10.2	BIT	* >		Value	%IX11.4	BIT		Value
		Channel 14.Value	%IX10.3	BIT	🐌		Value	%IX11.5	BIT		Value
		Channel 15.Value	%IX10.4	BIT	* >		Value	%IX11.6	BIT		Value
		Channel 16.Value	%IX10.5	BIT	* >		Value	%IX11.7	BIT		Value



Be careful with the areas assigned when passing the PLC part since they are modified by the system itself, I recommend verifying them and modifying them again according to what was previously configured



This also happens because the headend, the Coupler bus, has some input areas that are used as information and that end in this case in the %IX8.5 bit. In this case, when recovering the information downloaded from the existing configuration, the system continues from the free areas and therefore adjusts the values



Here we can see the Inputs area that is using the header. Therefore, this structure must be kept in mind when structuring the areas of the various I/O units that we have in the machine.

	🗮 DataLayerNode I/	O Mapping DataLayerNoo	de Parameters 🛛 Status 🏾 🌐 Information	n			
	Find	F	ilter Show all	-	🕂 Add FB	for IO Channel	→ Go to Instance
Occupation of the Inputs of the	Variable	Mapping	Channel	Address	Туре	Default Value	Current Value
	🖳 ··· 🧤		UP_Supply_periphery.UP_Voltage	%IW0	UINT		24141
XB_EC_12 (DataLayerNode)	🕸 - 🍫		UP_Supply_periphery.UP_Current	%IW2	UINT		91
	😟 🖓		UL_Supply_logic.UL_Voltage	%IW4	UINT		24172
	🗄 🦄		UL_Supply_logic.UL_Current	%IW6	UINT		162
	* >		State.UP_Undervoltage	%IX8.0	BIT		FALSE
	👋		State.UP_Overvoltage	%IX8.1	BIT		FALSE
	* >		State.UP_Overcurrent	%IX8.2	BIT		FALSE
	👋		State.UL_Undervoltage	%IX8.3	BIT		FALSE
	*		State.UL_Overvoltage	%IX8.4	BIT		FALSE
	*		State.UL_Overcurrent	%IX8.5	BIT		FALSE

Also in the ''DataLayerNode I/O Mapping'' of each of the modules, at least the ''Enabled 2'' option should be activated so that the I/O are updated automatically



Use parent device setting Enabled 1 (use bus cycle task if not used in any task) = = = Enabled 2 (always in bus cycle task)



Codesys, if you do not have any of the "Enabled" options activated, does not refresh the I/O areas, unless they are used in some part of the program, which obviously leads to errors if this issue is unknown, since it will surely we will think that the input or output cards are faulty

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ctrlX - Configuration of the ctrlX I/O – Online Connection

Now we can connect with the ctrlX to transfer the program or at least the configuration created up to that moment





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Annex Modbus communication

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ctrlX - Communication using Modbus

Modbus communication between the ctrlX and an XM is detailed in another manual. However, now the objective is to pass the state of the inputs to the XM and activate the outputs from the XM. In itself, the program will not differ much from what has already been mentioned in the previous manual, however, some aspects must be taken into account.

The system will use the Server - Client model



The Modbus operating modules that we are going to use allow the passage of up to four types of areas.

I / O Area	
65536 Bit Coil	
65536 Discrete Input	
65536 Word Input Register	
65536 Word Holding Register	

Although this is relatively true, the reality is that the assignment of areas in both teams differs slightly in the part called Coil. Therefore, care must be taken when transferring data.

I / O Area	ctrlX	
65536 Bit Coil	Byte	••
65536 Discrete Input	<u>Byte</u>	••
65536 Word Input Register	Word	•
65536 Word Holding Register	Word	
-		
I / O Area	XM	
<u>I/O Area</u> 65536 Bit Coil	XM Bool	• •
65536 Bit Coil 65536 Discrete Input	Bool	••
I/OArea 65536 Bit Coil 65536 Discrete Input 65536 Word Input Register	XM Bool Bool Word	• • •

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For this we are going to use the following libraries that must be installed on both computers





The data sent or received, as we have said, can be of four different types:

COIL	Coil L	Data		
DATA:	DATA: Opciones : Lectura / Escritura			
	Estructura :	Byte (ctrlX) / Bool (XM)		
	Definir tamaño del array con :	SIZEOF()		
	Representación :	1 Array / 8 bits		
	Opcional :	Uso de estructuras		

ctrlX arCoilData: ARRAY [0..7] OF BYTE;

XM arCoilData: ARRAY [0..7] OF BOOL;

INPUT	Input Data		
DATA:	Opciones :	Lectura	
	Estructura :	Byte (ctrlX) / Bool (XM)	
	Definir tamaño del array con :	SIZEOF()	
	Representación :	1 Array / 8 bits	
	Opcional :	Uso de estructuras	

ctrlX arInputData: ARRAY [0..7] OF BYTE;

XM arInputData: ARRAY [0..7] OF BOOL;

HoldingReg	isterData	HOLDING REGISTER	<i>REGISTER DATA:</i>	Regis	erData
Opciones :	Lectura / Escritura	These types of data allow the sending of structures and in them we can have different types of elements, Word, Int, Real, etc.		Opciones	: Lectura
Estructura :	Word			Estructura	: Word
Definir tamaño del array con :	SIZEOF()			Definir tamaño del array con	: SIZEOF()
Representación :	Word (16 bits)			Representación	: Word (16 bits)
Opcional :	Uso de estructuras 🛛 🧲	STRUCT		 Opcional 	: Uso de estructuras
stHoldingRegisterData, be written, we will use then outputs from the XM	Data:dutRegisterData; since they can n to activate the	TYPE dutRegisterData : arWord: ARRAY[0999]OF WORD; // 0 - 999 arInt: ARRAY[0999]OF INT; // 1000 - 19 arUint: ARRAY[0999]OF UINT; // 2000 - 29 arDint: ARRAY[0499]OF DINT; // 2000 - 39 arUdint: ARRAY[0499]OF DINT; // 3000 - 39 arUdint: ARRAY[0499]OF DINT; // 4000 - 49 arReal: ARRAY[0499]OF REAL; // 5000 - 59 arString: ARRAY[099]OF STRING(19);// 6000 - 69 END_STRUCT		9 1999 2999 3999 stRegisterDa 4999 5999 6999 M The Reg will be a inputs o	ata:dutRegisterData; gisterData as they are read only used to capture the image of the f the IO modules

Example of data passing at the HoldingRegisterData level, which also works for the RegisterData

The data must be extracted in individual groups, if we want to access the different parts of the generated structure, for this reason the same type of module is used, but each one for a different group.

ctrlX		XM		fbModBusReadHoldingRegisters_Word
= < stHoldingRegisterData	dutRegisterData	😑 < stHoldingRegisterData		fbModBusReadHoldingRegisters int
🗉 < arWord	ARRAY [0999] OF WORD	🗉 🔌 arWord		•
🗉 🧳 arInt	ARRAY [0999] OF INT	🗉 🛯 arInt 🖌	•	🖗 fbModBusReadHoldingRegisters_Uint
🗉 🧳 arUint	ARRAY [0999] OF UINT	🗉 📦 arUint 🛛 💕	Ŧ	fbModBusReadHoldingRegisters Dint
🗄 🛯 🎓 arDint	ARRAY [0499] OF DINT	🗉 📦 arDint 🛛 🖝		
🗉 < arUdint	ARRAY [0499] OF UDINT	🗉 🛯 arUdint 🛛 🖝		🛭 fbModBusReadHoldingRegisters_Udint
🗄 < arReal	ARRAY [0499] OF REAL	🗉 🗼 arReal 🛛 📥		hModBusPeadHoldingPegisters Peal
🗄 < arString	ARRAY [099] OF STRING(19)	🗉 🔌 arString 🛛 📥		
			E	fbModBusReadHoldingRegisters_String

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Program used in the ctrlX

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The control program used in the ctrlX is generated as follows





The way to "send" the input data and "receive" the outputs from the Modbus can be done as complicated as we want, but in my opinion the easiest thing is to do it as it appears in the image



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The relationship of the bytes with the words of the Register is visible in this image

Registers	Byte	Byte
IWO	0	1
IW1	2	3
IW2	4	5
IW3	6	7
IW4	8	9
IW5	10	11
IW6	12	13
IW7	14	15
IW8	16	17
IW9	18	19
<i>IW10</i>	20	21
IW11	22	23
<i>IW12</i>	24	25
<i>IW13</i>	26	27
<i>IW14</i>	28	29
<i>IW15</i>	30	31

HOLDING REGISTER DATA:

HoldingRegisterData			
Opciones :	Lectura / Escritura		
Estructura :	Word		
Definir tamaño del array con :	SIZEOF()		
Representación :	Word (16 bits)		
Opcional :	Uso de estructuras		

REGISTER DATA:

RegisterData		
Opciones : Lectura		
Estructura :	Word	
Definir tamaño del array con :	SIZEOF()	
Representación :	Word (16 bits)	
Opcional :	Uso de estructuras	



ctrlX - Control program used in the ctrlX

The ctrlX is used as a system server, leaving the program structure as follows





The Prog0070_0000_General POU calls the two Modbus communication control modules on the client side





The last module located in the ctrlX manages the control of the life bit that is sent to the XM and the error control in the communications coming from the XM



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Program used in the XM

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In the XM part and only for Modbus communications control we will use the following structure:

The structure of the Modbus communications area used in the XM is as follows:

ctrlX - Control program used in the XM

The sequence control module manages the steps for the activation of the modules and in case of an error in the communications it is restarted to be able to start again automatically.

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View of the sequence control, steps 0 and 1, as well as the communications activation module

View of Step 2, Reading the registers with the image of the inputs:

View Step 3, writing the registers for the activation of the outputs:

Step 3: Activate Writing of the "HoldingRegisterData"

The last of the Modbus control POUs is the control life bit. As in the ctrlX part, here we also activate a bit to send to the XM and manage the control of possible errors in the communication coming from ctrlX

Código

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Then we have the modules that are responsible for managing the input and output data

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ctrlX - Control program used in the XM

The instantiated modules control the read and write registers one by one, in order to facilitate the assignment of the bits that must be the image of the inputs and of the bits for the outputs used in the project.

The communication structure of the areas used in the Registerdata and HoldingRegisters are in Word format, so we must calculate at what point each read / write sector is initialized, especially if we want to send or receive more than 125 elements.

The first 4 areas of the structure are in Word format, so the real occupation corresponds 1 to 1. The following areas are in double word format, so the assigned value should be multiplied * 2, in this way we can adjust the values and know in which area we can act. From the example and with the structure shown, each area has a starting point

😑 🌒 stHoldingRegisterData	dutRegisterData	
🗉 🔌 arWord	ARRAY [0999] OF WORD	0
🗄 🖗 arInt	ARRAY [0999] OF INT	
🗉 🧳 arUint	ARRAY [0999] OF UINT	2000
🗉 🧳 arDint	ARRAY [0499] OF DINT	3000
🗉 < arUdint	ARRAY [0499] OF UDINT	<u>4000</u>
표 < arReal	ARRAY [0499] OF REAL	5000
🗉 < arString	ARRAY [099] OF STRING(19)	6000

The modules only allow sending 125** elements each time through the "Quantity" parameter, if we have an area of 1000 words, for example, we must take into account that access should be made in eight blocks, modifying in this case the value assigned in "FirstRegister"

	Start	End
1	0	124
2	125	249
3	250	374
4	375	499
5	500	624
6	625	749
7	750	874
8	875	999

**In some cases it has been observed that only a maximum of 100 elements could be sent, so in the communication example used, we are using a 100 and that is why we use Word[99].15 as the life bit

ctrlX - Video

Control modules	in XM		×	HoldingPogistorData (
🗧 😳 Application 🛗 👒 🧐 🕨 🔳 🔍 🖷	,= •= °= % • */	-Van ()	- «»- P	
g0070_0000_General + PlcProg + Prog0000_0003_Blinks	+ Prog0000_0000_General	+ GVL_CtrlModbus	n ₹ ×	
IndraMotionMlc1.Application.Prog0005_0001_ControlIO				CtrlXCorePL ControlIQ
Application (Plot Program (Program) O070_0000_General + PlcProg + Program(Program) Foression F	+ Prog0000_0000_General + Prog0000_0000_General Type Value ftctrlXIO ftctrlXIO ftctrlXIO BOOL FALSE BIOL FALSE BIOL FALSE BIOL FALSE BIOL FALSE FIL	FILES PLASE PL		Devices
72155 - 555109_1R 72155 - 555109_1R 72455 - 555109_1R 72455 - 555107_IR 72455 - 55511_IR 72455 -	bBit05_00t = 7435 bBit05_00t = 7435 bBit07_00t = 7435 bBit11_00t = 7435 bBit11_00t = 7435 bBit12_00t = 7435 bBit12_00t = 7435 bBit14_00t = 7435 bBit15_00t = 7435 bBit16_00t = 7435 bBit16_00t = 7435 bBit16_00t = 7435 bBit16_00t = 7435	RegisterData.arWord(6	5] 0	

ngRegisterData (Outputs in ctrlX)										
▼ ₽	×	ry Manager	Prog0005_0001_Ctrl	X_Inputs	8					
10	•	Device.Application.GVL_Structures								
ected] (ctrlX CORE)			Type	Value	Ī					
ation [run]		gisterData	dutRegisterData							
ckFunctions		oldingRegisterData	dutRegisterData							
005_CtrlIO		arWord	ARRAY [0999] OF							
0005 0000 General (PRG)		arWord[0]	WORD	0						
Prog0005_0001_CtrlX_Inputs (PRG)	arWord[1]	WORD	0							
Drag0005_0003_CtrlV_Outputs (DBC)		arWord[2]	WORD	0						

arWord[3]

arWord[4]

arWord[5]

arWord[6]

arWord[7]

arWord[8]

arWord[9]

arWord[10]

arWord[11]

arWord[12]

arWord[13]

arWord[14]

arWord[15]

arWord[16]

arWord[17]

arWord[18]

arWord[19]

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arWord[21]

arWord[22]

arWord[23]

arWord[24]

arWord[25]

arWord[26]

arWord[27]

▲ prillord[101

Download Description WORD

MODD Messages - Total 0 error(s), 15 warning(s), 6 message(s)

A core dump created on the 19/03/2022 ...

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Project

8192

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Notes:

- It is recommended to use a sequence of steps to carry out a controlled sending of the data.
- If this is not done, errors may occur.
- The communication must be associated with a standard Task and never with a Sercos task.
- The sequence used in the XM part manages the control of the reads and the error in the initial communication.
- This programming is done my way and it is obvious that the final goal can be achieved in many ways.
- This is just a small example of Modbus communication and some program changes may be required to get the best results.
- As we have some areas for reading and writing and others for reading only, we can use them separately and in this way manage the data sent and the data received.

Thanks for your attention

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